CLAIMS

What is claimed is:

1. A method for determining the logic state of a memory cell in a magnetic tunnel junction (MTJ) memory device, comprising the steps of:

applying a first bias voltage to the cell;

measuring a current flowing through the cell at the first bias voltage;

applying a second bias voltage to the cell, the second bias voltage being different from the first bias voltage;

measuring a current flowing through the cell at the second bias voltage;

determining a ratio of the current flowing through the cell at the first bias voltage with the current flowing through the cell at the second bias voltage; and

comparing the determined ratio to a predetermined value.

2. The method of claim 1, wherein the second bias voltage is less than the first bias voltage.

3. The method of claim 1, wherein the second bias voltage is greater than the first bias voltage.

4. The method of claim 1, wherein the second bias voltage is on the order of 1/3 of the first bias voltage.

5. The method of claim 1, wherein the predetermined value is determined by the steps of:

applying a first bias voltage to a reference MTJ memory cell, the state of said reference device being known;

measuring a current flowing through the reference cell at the first bias voltage;

applying a second bias voltage to the reference cell, the second bias voltage being different from the first bias voltage;

measuring a current flowing through the reference cell at the second bias voltage; and

determining a ratio of the current flowing through the reference cell at the first bias voltage with the current flowing through the reference cell at the second bias voltage.

6. The method of claim 1, wherein the MTJ device is a magnetic random access memory (MRAM).

7. The method of claim 6, wherein the MRAM is an MRAM array.

8. A system for determining the logic state of a memory cell in a magnetic tunnel junction (MTJ) memory device, comprising:

a biasing circuit configured to supply at least two different biasing voltages to the cell;

a sensing circuit configured to measure the current flowing through the cell at each of the at least two different biasing voltages; and

a processing element configured to determine a ratio of the current flowing through the cell at a first one of the at least two different biasing voltages to the current flowing through the cell at a second one of the at least two different biasing voltages and to compare the ratio to a predetermined value.

9. The system of claim 8, wherein the biasing circuit, the sensing circuit, the processing element and the MTJ device are fabricated as an application specific integrated circuit (ASIC).

10. The system of claim 8, wherein the biasing circuit is a voltage supply.

11. The system of claim 8, wherein the sensing circuit is an ammeter.

12. The system of claim 8, further comprising a reference MTJ memory cell having a known state.

13. The system of claim 8, wherein the MTJ device is a magnetic random access memory (MRAM).

14. The system of claim 10, wherein the MRAM is an MRAM array.

15. A computer readable medium for facilitating the determination of the logic state of a memory cell in a magnetic tunnel junction (MTJ) memory device, comprising:

logic configured to apply a first bias voltage to the cell and a second bias voltage to the cell, the second voltage being different from the first bias voltage;

logic configured to measure a first current flowing through the cell at the first bias voltage and a second current flowing through the cell at the second bias voltage;

logic configured to determine a ratio of the first current to the second current and compare the ratio to a predetermined value.

16. The computer readable medium of claim 15, wherein the second bias voltage is less than the first bias voltage.

17. The computer readable medium of claim 15, wherein the second bias voltage is more than the first bias voltage.

18. The computer readable medium of claim 15, wherein the second bias voltage is on the order of 1/3 of the first bias voltage.

19. The computer readable medium of claim 15, wherein the predetermined value is determined by:

logic configured to apply a first bias voltage and a second bias voltage to a reference MTJ memory cell having a known logic state;

logic configured to measure a first current flowing through the reference cell at the first bias voltage and a second current flowing through the reference cell at the second bias voltage; and

logic configured to determine a ratio of the current flowing through the reference device at the first bias voltage with the current flowing through the reference device at the second bias voltage.

20. The computer readable medium of claim 15, wherein the MTJ device is a magnetic random access memory (MRAM).